REMARKS/ARGUMENTS

In the April 21, 2005 Office Action, the Examiner rejected Claims 1-3, 6, 8-9 under 35 USC § 102(e) as being unpatentable over Harumoto (US Patent No. 6,460,097); and Claim 4-5

5   under Iwasaki (US Patent No. 6,198,876). The Examiner also rejected Claims 7 and 10 under 35 USC § 103(a) over Harumoto in view of Iwasaki. Applicants thank Examiner Casiano and Primary Examiner Gaffin for the telephone interview that was conducted on June 16th, 2005, and a summary of the interview is provided below. Applicants have amended Claims 1-2 and 4-7, 9-10, cancelled claims 8 and 11, and added new Claim 12. Claims 1-7, 9-10 and 12 are now pend-

10   ing of which Claims 1, 4, 6 and 9 are independent claims. Applicants respectfully request reconsideration of the patentability of the claims of the present application in view of the amendments and the following remarks.

DRAWING OBJECTIONS

The Examiner had objected to the following figures:

15   Figure 1B: 108J, 108G, 108I and 108F

Applicants have amended paragraph [0038] to reference 108F and 108I in the specification. Applicants also submit substitute Figure 1B where reference to 108J and 108G has been removed.

Figure 3: 301

20   Applicants have amended paragraph [0046] to reference 301 in the specification.

Figure 4: 402

Applicants have amended paragraph [0047] to reference 402 in the specification.

Applicants respectfully request acceptance of the amendments and withdrawal of this objection.

25   ## TITLE OF THE INVENTION

Applicants have changed the Title of The Invention and request withdrawal of this objection.

SUMMARY OF TELEPHONE INTERVIEW

The undersigned conducted a telephone interview with Examiner Casiano and Primary Examiner Gaffin. The primary reference Harumoto was discussed with respect to amended Claims 1 and Claim 6. The undersigned explained how the present invention was different from

5   Harumoto. An agreement was reached that amended Claims 1 and 6 appear to overcome Harumoto but the further search may be conducted after an official response is submitted.

Rejection Under 35 USC § 102(e)

Claim 1:

The Examiner cites:

10   Regarding Claim 1, Harumoto et. al. teaches a method for processing data by a storage controller with a buffer controller coupled to a buffer memory (see Abstract; Figure 1). The reference teaches the steps of evaluating incoming data block size (see Abstract; col. 4, lines 58-62); determining the incoming data requires padding (see col. 4, line 63); and padding incoming data such that the incoming data can be processed by the buffer controller (see "padding so to

15   have a fixed size K; col. 4, line 64). (Office Action, Page 3, Para 5)

Harumoto fails to disclose the elements of Claim 1. In particular, Harumoto, fails to disclose, a method for processing incoming data from a host system and received by a storage controller having a buffer controller coupled to a buffer memory. The method includes evaluating data block length in real time for the incoming data that is received by a first FIFO

20   based memory in a first channel of the buffer controller, wherein a first channel controller of the buffer controller evaluates the data block length using a data length counter and a bit value set up by storage controller firmware in a first channel controller register allows the buffer controller to process any MOD size data block ; determining if the incoming data requires padding based on whether alignment of data received by the buffer controller from the host system is different

25   from alignment of data used by the buffer controller to process data, which is sent to the storage device; and padding incoming data such that the incoming data can be processed by the buffer controller"(Amended Claim 1).

Support for the amendments to Claim 1 are provided in the specification as follows:

Evaluating <u>block length in real time for the incoming data that is received by a first FIFO</u> <u>based memory in a first channel of the buffer controller, wherein a first channel controller of the</u> <u>buffer controller evaluates the data block length using a data length counter and a bit value set</u>

5   <u>up by storage controller firmware in a first channel controller register allows the buffer controller</u> <u>to process any MOD size data block :</u> See Paragraphs [0040 (c)], [0042],[0044], [0046] [0049] and [0051].

Determining if the incoming data requires padding <u>based on whether alignment of data</u> <u>received by the buffer controller from the host system is different from alignment of data used by</u>

10   <u>the buffer controller to process data, which is sent to the storage device:</u> See paragraphs [0046] and [0051].

Harumoto, discloses "a read buffer (pre-reading buffer 103)" in a data stream output apparatus. A "data stream is read from a storage medium, and a memory is provided for storing a time table Mt indicating the position and size of the data block to be sent out to the external de-

15   vice every given period (f) in the data stream, the data block including motion picture data to be decoded by the external device every given period(f). Further a send buffer 110 is provided for storing the data stream to be sent out to the external device via the digital interface." (Harumoto, Abstract) Harumoto provides "a controller for controlling the outputting of the data stream stored by the read buffer 13 from the send buffer 110 to the external device via digital interface,

20   so as to have a fixed size (K) when the size (Sm) of transmit data block is not equal to the fixed size (K), controls the outputting of the resultant data block from the send buffer 110 to the external device via the digital interface." (Harumoto, Abstract).

It is Harumoto's object "to provide a data stream output apparatus which can read out variable encoded data from such storage media as hard disk and DVD while maintaining continuity and permits push-type transfer to a network and that transfers data to a network system while efficiently shaping the data to a fixed size". (Harumoto, Col. 3, lines 52-60). Harumoto

5   performs this by using two buffers (pre-read buffer 103 and send buffer 110) and maintaining a timetable Mt. This is different from the process steps of amended Claim 1 as discussed during the telephone interview and explained below.

In particular, as stated in amended Claim 1, a FIFO in the first channel of the buffer controller receives data from the host system (not from the storage device). By setting a bit in a first

10   controller register, the buffer controller can be set in a mode to receive an MOD size data block. A first channel controller using a data length counter in real time determines if the data alignment of the received data is different from the data alignment that is used by the buffer controller to process the data. If the data alignment is different then the data is padded. This allows the buffer controller/storage controller to process data blocks of any alignment received from a host

15   system. This is different from Harumoto.

Based on the foregoing reasons, Applicants respectfully submit that Claim 1 is patentably distinguished over Harumoto. Therefore, Applicants respectfully request allowance of amended Claim 1.

Claims 2-3:

20   Claims 2-3 depend from Claim 1 and are thus patentably distinguished over Harumoto for at least the same reasons provided above with respect to Claim 1. Therefore, Applicants respectfully request allowance of Claims 2-3.

Claim 4-5:

The Examiner rejected Claim 4-5 based on Iwasaki stating:

"Regarding claim 4, Iwasaki et al. teaches a method for reading data (Abstract), including a buffer memory and controller (see Figure 8). The reference teaches determining if any pads need to be removed from the data and removes pads from the data (see col. 3, lines 9-18; "removing padding data", col., 4, lines 66-67; col. 5, lines 1-4, 41). (Office Action, Page 5, Para 6).

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Iwasaki fails to disclose the elements of amended Claim 4. In particular, Iwasaki fails to disclose, a method for sending data from a storage device to a host system via a buffer memory

10   that is operationally coupled to a storage controller, which is regulated by a buffer controller.

Iwasaki fails to disclose the process steps of: "determining if any pads needs to be removed from the data before the data is read from the buffer memory; wherein a first channel controller of the buffer controller evaluates the data in real time and if data alignment is different from a data alignment used by an interface that sends the data to the host system, then the first channel con-

15   troller determines that padding needs to be removed from the data; and a bit value set up by stor-age controller firmware in a first channel controller register allows the buffer controller to proc-ess any MOD size data block; removing pads from the data read from the buffer memory; and continuing to determine if any pad needs to be removed and removing the pad if data alignment of the data stored in the buffer memory is different from the data alignment used by the interface,

20   until a last block of data has been read from the buffer memory." (Amended Claim 4)

Iwasaki discloses a disk array device 10 that includes a disc array unit 11 for accessing video data of 163840 bytes and audio data of 8192 bytes. A data adjustment unit 25 for append-ing nonsensical data (padding data) to a superfluous portion produced by non-coincidence be-tween the size of 3584 bytes and the data size of 4096 bytes during recording and for removing

25   the padding data during reproduction for taking out the data. (Iwasaki, Col. 4, lines 60-67 and Col. 5, lines 1-4). The data adjustment unit 25 has a padding data processing circuit 26 for con-

trolling a SCSI interface circuit 27 and a buffer memory 28 by a direct memory accessing for

appending or removing the padding data to or from the AV data. (Iwasaki, Col. 5, lines 38-42).

Iwasaki discloses a padding data processing circuit 26 that "includes a clock generating

circuit 31 for generating reference clock signals, and a readout clock generating circuit 32 for

5   generating data readout clock signals based on clock signals from clock generating circuit 31.

The padding data processing circuit 26 also includes a data readout control circuit 33 for causing

data to be read from the SCSI interfacing circuit 27 to the buffer memory 28 by the above data

readout clock signals and a memory write control circuit 34 responsive to the clock signals from

the clock signals from the clock generating circuit 31 to control writing of the AV data in the

10   buffer memory." (Iwasaki, Col. 5, lines 46-57).

Iwasaki is different from the method disclosed in amended Claim 4. For example, Iwa-

saki does not disclose a first channel controller of the buffer controller that evaluates data and if

data alignment is different from a data alignment used by an interface that sends the data to the

host system, and then the first channel controller determines that padding needs to be removed

15   from the data.

Claim 4 is patentably distinguished over Iwasaki for at least the same reasons provided

above. Therefore, Applicants respectfully request allowance of Claim 4.

Claim 5 depends from Claim 4 and is thus patentably distinguished over Iwasaki for at

least the same reasons provided above with respect to Claim 4. Therefore, Applicants respect-

20   fully request allowance of Claim 5.

Claim 6:

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The Examiner rejected Claim 6 over Harumoto. Claim 6 is patentably distinguished over Harumoto for at least the same reasons provided above with respect to Claim 1. Therefore, Applicants respectfully request allowance of Claim 6.

Claim 9 and 11:

5   The Examiner rejected Claim 9 over Harumoto. Claim 9 is patentably distinguished over Harumoto for at least the same reasons provided above with respect to Claim 1. Therefore, Applicants respectfully request allowance of Claim 9.

Claim 11 is rejected over Harumoto. Claim 11 depends from Claim 9 and is thus patentably distinguished over Harumoto for at least the same reasons provided above with respect to

10   Claim 9 (and Claim 1). Therefore, Applicants respectfully request allowance of Claim 11.

Claim 7 and 10:

The Examiner rejected Claims 7 and 10 over Harumoto in view of Iwasaki. Claim 7 depends from Claim 6, while Claim 10 depends from Claim 9. Assuming arguendo that Harumoto

15   and Iwasaki can be combined, the combination does not remove deficiency of Harumoto (described above with respect to Claim 1) and Iwasaki (described above with respect to Claim 4). Therefore, Applicants respectfully request allowance of Claims 7 and 11.

New Claim 12: Claim 12 is also allowable over Harumoto and/or Iwasaki based on the reasons provided above with respect to Claim 1 and Claim 4. Therefore, Applicants respectfully

20   request allowance of Claim 12

CONCLUSION

For the foregoing reasons, Applicants believe Claims 1-7, 9-10 and 12 are allowable, and a notice of allowance is respectfully requested. If the Examiner has any questions regarding the application, the Examiner is invited to call the undersigned Attorney at (949)-389-6532.

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Dated: _July 15, 2005_   Respectfully submitted,

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15   I hereby certify that this correspondence is being faxed to the USPTO, fax number 703-872-9306 to on

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20   _____   _July 15_ , 2005
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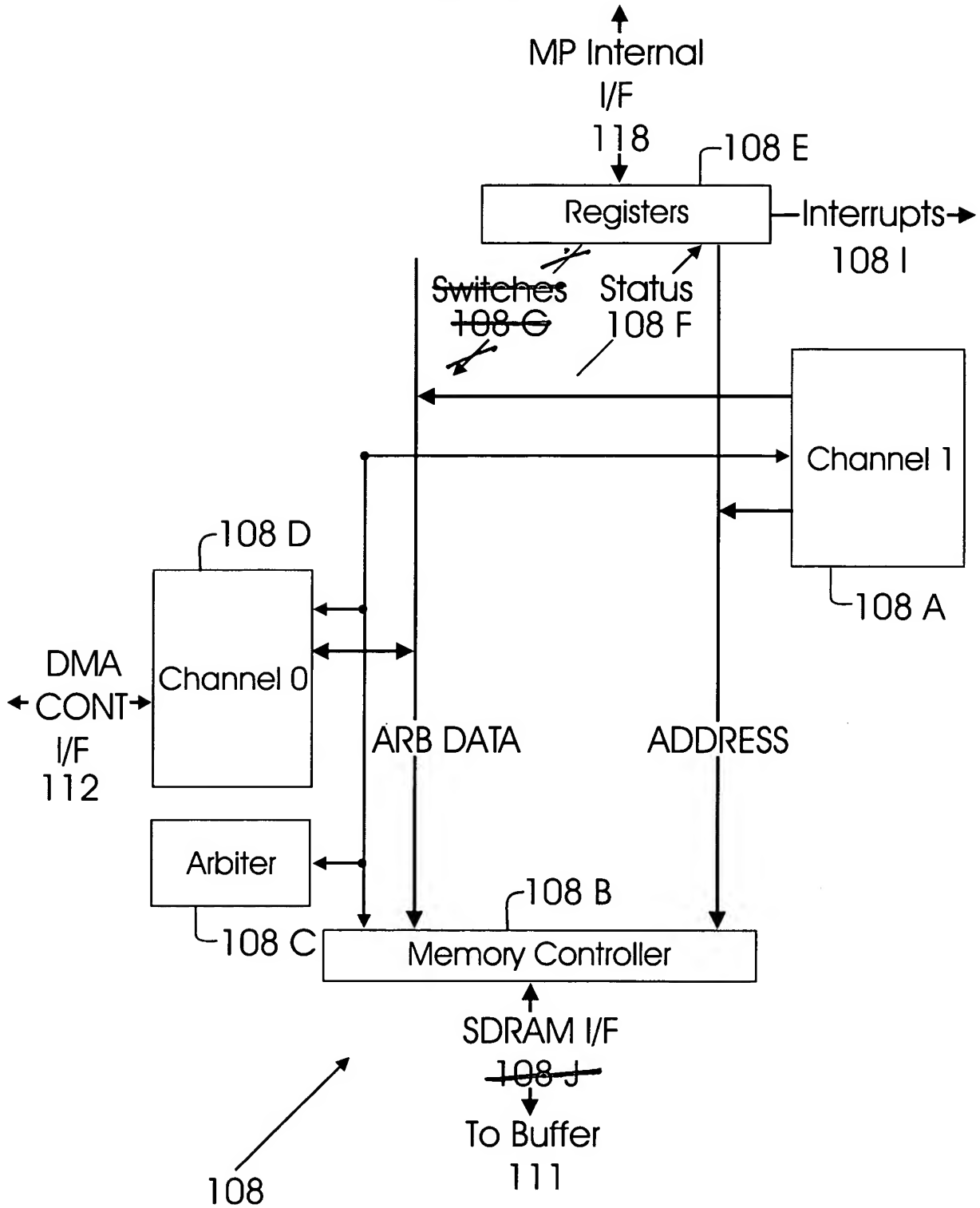
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FIGURE 1B